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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,785	09/29/2003	Atsushi Date	03500.017602.	7534

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	
MAIL DATE	**DELIVERY MODE**
12/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,785	DATE, ATSUSHI	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 7-9 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE and Amendment as received on 9/18/2007.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Kirkwood, U.S. Patent No. 6,810,460.

5. Referring to claim 1, Kirkwood has taught a processor system on a single semiconductor substrate (Fig.1, component 10), wherein the processor system is provided with a built-in processor (Fig.1, component 12), a memory controller (a system inherently has memory and consequently, it also has a controller to control memory), an external bus interface that can connect an external processor from outside of a single semiconductor substrate (Fig.1, at least one of components 24, 26, and 28), a processor bus which is connected with the built-in

processor and the external bus interface (Fig.1, component 20), and a connection unit that mutually connects the memory controller and the processor bus (processors are inherently connected to memory so that instructions may be obtained for execution), wherein first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, and wherein one of the first mad second enable signals is asserted while the other one of the first and second enable signals is deasserted, so that issuance of a request for using the processor bus from one of the built-in processor and the external bus interface to which the asserted enable signal is input can be suppressed and the other one of the built-in processor and the external bus interface can use the processor bus exclusively. See Fig.2, column 3, lines 1-3, and column 3, lines 26-38, and note the HREADY signal coupled to the built-in processor. This signal, while low, prevents the built-in CPU from requesting the bus because a transfer is being performed by the external device using the bus. Also, see the HBUSREQx signal of column 3, lines 49-59. This signal allows the built-in processor to use the bus while preventing the external device from issuing a request to use the bus.

6. Referring to claim 3, Kirkwood has taught the processor system according to claim 1, wherein the connection unit includes a common bus. See Fig.1.

7. Referring to claim 7, Kirkwood has taught the processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the connection unit. See Fig.1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 4, and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkwood.

10. Referring to claim 2, Kirkwood has taught the processor system according to claim 1. Kirkwood has not explicitly taught that the connection unit is a crossbar switch. However, crossbar switches and their advantages are well known and accepted in the art. A crossbar switch is useful because as the traffic between any two devices increases, it does not affect traffic between other devices. In addition, it is much more scalable than a traditional bus. Consequently, to reduce traffic and increase scalability, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kirkwood such that the connection unit is a crossbar switch.

11. Referring to claim 4, Kirkwood has taught the processor system according to claim 1. Kirkwood has not taught a second built-in processor connected to the connection unit on the semiconductor substrate. However, systems having multiple processors or being scaled to include multiple processors is known in the art and advantageous because more processors yield more processing power, and throughput. Consequently, in order to increase performance, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify

Kirkwood to include a second built-in processor connected to the connection unit on the semiconductor substrate.

12. Referring to claim 8, Kirkwood has taught the processor system according to claim 1. Kirkwood has not taught that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller. However, it is knows that a single program may be broken up into pieces to be executed by multiple processors, thereby speeding up execution of that single program. Consequently, when the FPGA 30 (Fig.1) of Kirkwood is programmed to be a processor, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kirkwood such that the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

13. Referring to claim 9, Kirkwood has taught the processor system according to claim 1. Kirkwood has not taught an image data transfer bus connected with the connection unit, nor has Kirkwood taught an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate. However, image processing is well known in the art, and in order to obtain image processing functionality in the system of Kirkwood, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kirkwood to include an image data transfer bus and an image output device interface or image input device interface so that images may be transferred to and from the processor for or after processing.

Response to Arguments

14. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Nutter, Jr. et al., U.S. Patent No. 4,059,851, has taught a priority network for devices coupled by a common bus wherein a highest priority device requesting bus access prevents all lower priority devices from gaining access to the common bus until the highest priority device completes its data transfer.

Kumar et al., U.S. Patent No. 5,287,464, has taught an off-chip processor sharing a bus with an on-chip processor.

Lee at al., U.S. Patent No. 6,973,526, has taught allowing an external microcontroller to access internal configuration registers.

Larson et al., U.S. Patent No. 5,524,235, has taught a system for arbitrating access to memory with dynamic priority assignment, wherein peripheral requests are prevented.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
November 27, 2007